



Docket No. 034299-336

TECHNOLOGY CEXTER 2000

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT:

Pelloie, et al.

SERIAL NO.:

09/890,120

FILING DATE:

July 27, 2001

TITLE:

DYNAMIC THRESHOLD VOLTAGE MOS TRANSISTOR

FITTED WITH A CURRENT LIMITER, AND PROCESS FOR

MAKING THE SAME

EXAMINER:

Edgardo Ortiz

ART UNIT:

2815

CERTIFICATE OF MAILING

I hereby certify that this paper is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Commissioner for Patents, Washington, DC 20231, on the date printed below:

Diane Morse

COMMISSIONER FOR PATENTS WASHINGTON, D.C. 20231

TRANSMITTAL LETTER

Enclosed for filing are the following documents:

- Request for Extension of Time; and 1.
- 2. Response.

Enclosed is our check in the amount of \$110.00 for the filing fee - Fee Code 115. The Commissioner is hereby authorized to charge our Deposit Account No. 50-1698 for any additional fees for filing the above-noted document, including any fees required

under 37 CFR § 1.136 for any necessary Extension of Time to make the filing of the attached document timely. A duplicate copy of this page is enclosed.

Respectfully submitted,

THELEN REID & PRIEST LLP

William E. Winters

Reg. No. 42,232

Dated: September 18, 2002

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Date: 9 19 02

Name

Diane Morse

BOX NON-FEE AMENDMENT COMMISSIONER FOR PATENTS WASHINGTON, D.C. 20231

RESPONSE

This paper is responsive to the Office Action dated August 9, 2002.

REMARKS

The present application stands subject to a restriction requirement. According to the restriction requirement, claims 1-11 have been delineated as being directed at a first invention identified as Group I drawn to a semiconductor device, classified in class 257, subclass 347 and claims 12-24 have been delineated as being directed at a second